embOS

Real-Time
Operating System

CPU & Compiler
specifics for CortexM
using TI Code Composer
Studio

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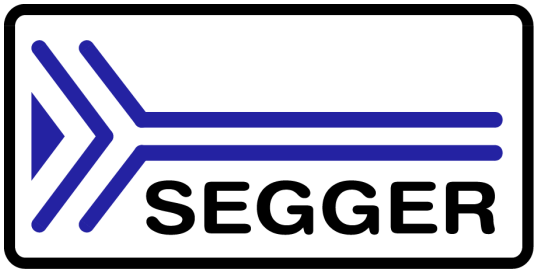
Software version 4.24
Revision: 0
Date: July 19, 2016



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Manual versions

This manual describes the current software version. If any error occurs, inform us and we will try to assist you as soon as possible.
Contact us for further information on topics or routines not yet specified.

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Software	Revision	Date	By	Description
4.24	0	160719	RH	Chapters "RTT and SystemView" and "Vector Floating Point support" added.
4.14	0	151124	MC	Update to latest software version.
3.88e	0	130920	TS	First version.

About this document

Assumptions

This document assumes that you already have a solid knowledge of the following:

- The software tools used for building your application (assembler, linker, C compiler)
- The C programming language
- The target processor
- DOS command line

If you feel that your knowledge of C is not sufficient, we recommend The C Programming Language by Kernighan and Richie (ISBN 0-13-1103628), which describes the standard in C-programming and, in newer editions, also covers the ANSI C standard.

How to use this manual

This manual explains all the functions and macros that the product offers. It assumes you have a working knowledge of the C language. Knowledge of assembly programming is not required.

Typographic conventions for syntax

This manual uses the following typographic conventions:

Style	Used for
Body	Body text.
`Keyword`	Text that you enter at the command-prompt or that appears on the display (that is system functions, file- or pathnames).
`Parameter`	Parameters in API functions.
`Sample`	Sample code in program examples.
`Sample comment`	Comments in programm examples.
Reference	Reference to chapters, sections, tables and figures or other documents.
GUIElement	Buttons, dialog boxes, menu names, menu commands.
Emphasis	Very important sections.

Table 2.1: Typographic conventions

SEGGER Microcontroller GmbH & Co. KG develops and distributes software development tools and ANSI C software components (middleware) for embedded systems in several industries such as telecom, medical technology, consumer electronics, automotive industry and industrial automation.

SEGGER's intention is to cut software development time for embedded applications by offering compact flexible and easy to use middleware, allowing developers to concentrate on their application.

Our most popular products are emWin, a universal graphic software package for embedded applications, and embOS, a small yet efficient real-time kernel. emWin, written entirely in ANSI C, can easily be used on any CPU and most any display. It is complemented by the available PC tools: Bitmap Converter, Font Converter, Simulator and Viewer. embOS supports most 8/16/32-bit CPUs. Its small memory footprint makes it suitable for single-chip applications.

Apart from its main focus on software tools, SEGGER develops and produces programming tools for flash micro controllers, as well as J-Link, a JTAG emulator to assist in development, debugging and production, which has rapidly become the industry standard for debug access to ARM cores.

Corporate Office:
http://www.segger.com

United States Office:
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EMBEDDED SOFTWARE (Middleware)

emWin
Graphics software and GUI
emWin is designed to provide an efficient, processor- and display controller-independent graphical user interface (GUI) for any application that operates with a graphical display.

embOS
Real Time Operating System
embOS is an RTOS designed to offer the benefits of a complete multitasking system for hard real time applications with minimal resources.

embOS/IP
TCP/IP stack
embOS/IP a high-performance TCP/IP stack that has been optimized for speed, versatility and a small memory footprint.

emFile
File system
emFile is an embedded file system with FAT12, FAT16 and FAT32 support. Various Device drivers, e.g. for NAND and NOR flashes, SD/MMC and CompactFlash cards, are available.

USB-Stack
USB device/host stack
A USB stack designed to work on any embedded system with a USB controller. Bulk communication and most standard device classes are supported.

SEGGER TOOLS

Flasher
Flash programmer
Flash Programming tool primarily for micro controllers.

J-Link
JTAG emulator for ARM cores
USB driven JTAG interface for ARM cores.

J-Trace
JTAG emulator with trace
USB driven JTAG interface for ARM cores with Trace memory. supporting the ARM ETM (Embedded Trace Macrocell).

J-Link / J-Trace Related Software
Add-on software to be used with SEGGER's industry standard JTAG emulator, this includes flash programming software and flash breakpoints.

Table of Contents

Chapter 4

Using embOS

The following chapter describes how to start with and use embOS for Cortex-M and TI Code Composer Studio. You should follow these steps to become familiar with embOS for Cortex-M and CCS.

4.1 Installation

embOS is shipped as a zip-file in electronic form.

To install it, proceed as follows:

Extract the zip-file to any folder of your choice, preserving the directory structure of this file. Keep all files in their respective sub directories. Make sure the files are not read only after copying.

Assuming that you are using TI Code Composer Studio to develop your application, no further installation steps are required. You will find a lot of prepared sample start projects, which you should use and modify to write your application. So follow the instructions of section “First steps” on page 11.

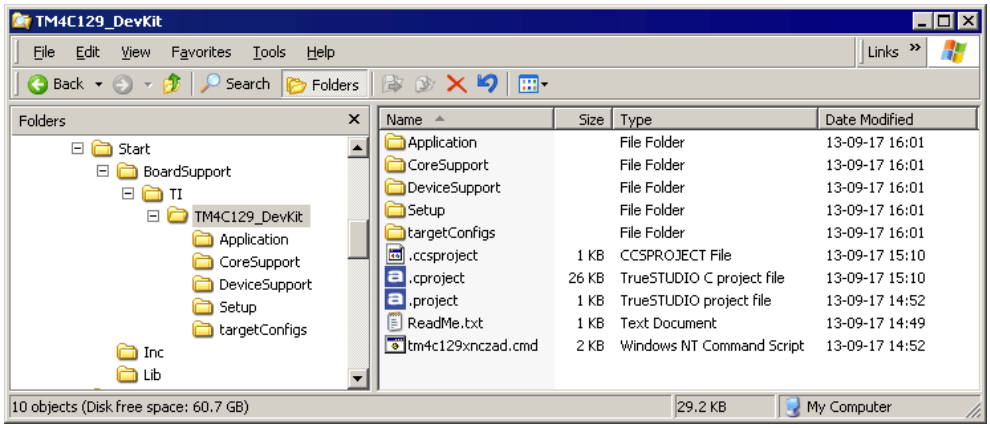
You should do this even if you do not intend to use the project manager for your application development to become familiar with embOS.

If you will not work with the TI CCS, you should: Copy either all or only the library-file that you need to your work-directory. This has the advantage that when you switch to an updated version of embOS later in a project, you do not affect older projects that use embOS also. embOS does in no way rely on the TI CCS it may be used without the project manager using batch files or a make utility without any problem.

4.2 First steps

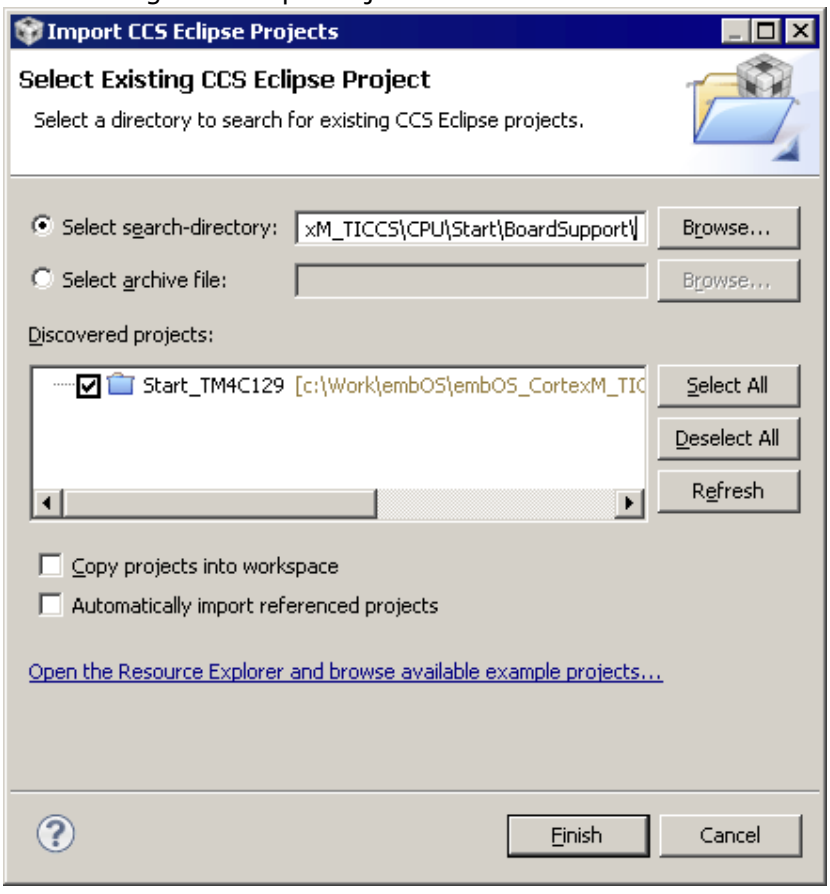
After installation of embOS you can create your first multitasking application. You have received ready to go sample TI CCS project files and it is a good idea to use one of these as a starting point of all your applications.
Your embOS distribution contains one folder "Start\BoardSupport" which contains the sample project files and every additional files used to build your application.

For the first step, you may use the project for TI TM4C129 CPU:



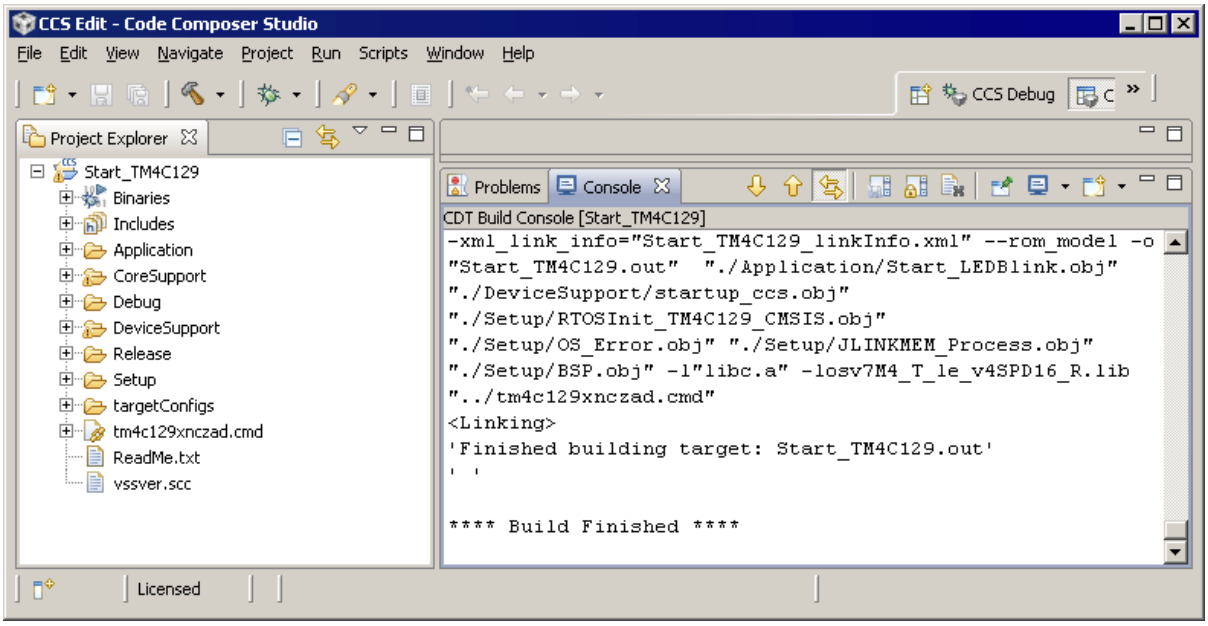
To get your new application running, you should proceed as follows:

- Create a work directory for your application, for example c:\work
- Copy the whole folder **Start** which is part of your embOS distribution into your work directory.
- Clear the read-only attribute of all files in the new **Start** folder.
- Start TI Code Composer Studio and import the project with Menu->Project->Import existing CCS Eclipse roject.



- Build the start project. It should be build without any error or warning messages.

After generating the project of your choice, the screen should look like this:



For additional information you should open the `ReadMe.txt` file which is part of every specific project. The ReadMe file describes the different configurations of the project and gives additional information about specific hardware settings of the supported eval boards, if required.

4.3 The example application OS_StartLEDBlink.c

The following is a printout of the example application `OS_StartLEDBlink.c`. It is a good starting point for your application. (Note that the file actually shipped with your port of embOS may look slightly different from this one.)

What happens is easy to see:

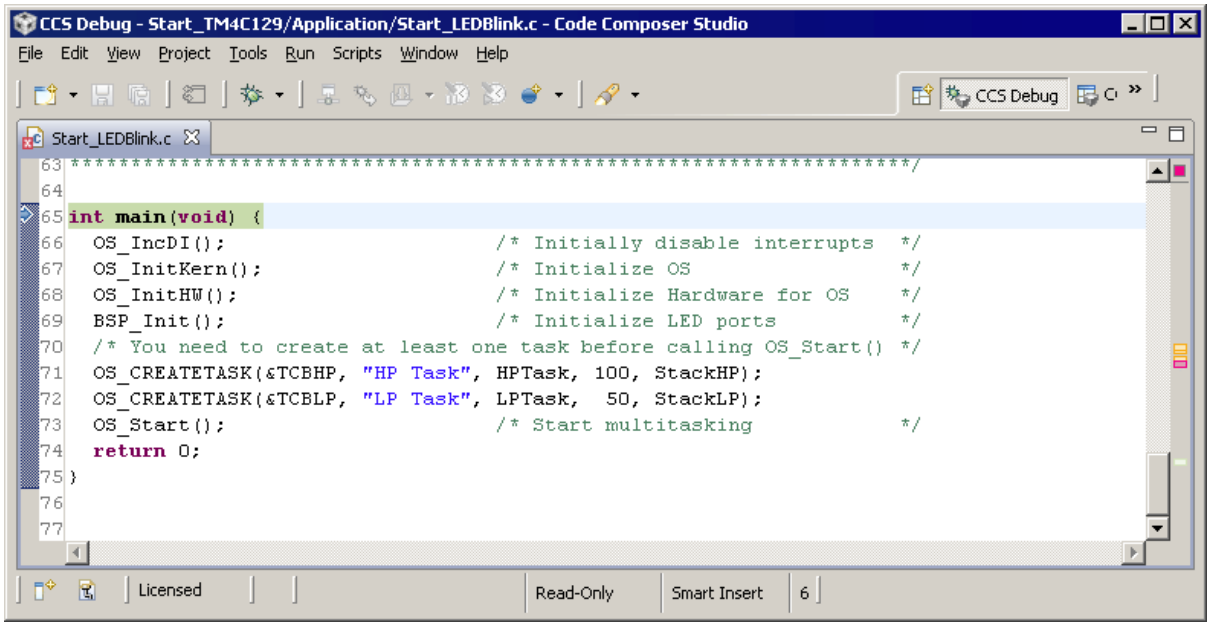
After initialization of embOS; two tasks are created and started.
The two tasks are activated and execute until they run into the delay, then suspend for the specified time and continue execution.

```
/*********************************************************************
*                 SEGGER Microcontroller GmbH & Co. KG               *
*                     The Embedded Experts                           *
**********************************************************************
File    : OS_StartLEDBlink.c
Purpose : embOS sample program running two simple tasks, each toggling
          a LED of the target hardware (as configured in BSP.c).
--------- END-OF-HEADER ------------------------------------------------
*/

#include "RTOS.h"
#include "BSP.h"

static OS_STACKPTR int StackHP[128], StackLP[128];   /* Task stacks */
static OS_TASK         TCBHP, TCBLP;         /* Task-control-blocks */

static void HPTask(void) {
  while (1) {
    BSP_ToggleLED(0);
    OS_Delay (50);
  }
}

static void LPTask(void) {
  while (1) {
    BSP_ToggleLED(1);
    OS_Delay (200);
  }
}

/*********************************************************************
*
*       main()
*/
int main(void) {
  OS_IncDI();                      /* Initially disable interrupts  */
  OS_InitKern();                   /* Initialize OS                 */
  OS_InitHW();                     /* Initialize Hardware for OS    */
  BSP_Init();                      /* Initialize LED ports          */
  /* You need to create at least one task before calling OS_Start() */
  OS_CREATETASK(&TCBHP, "HP Task", HPTask, 100, StackHP);
  OS_CREATETASK(&TCBLP, "LP Task", LPTask,  50, StackLP);
  OS_Start();                      /* Start multitasking            */
  return 0;
}

/****** End Of File *************************************************/
```

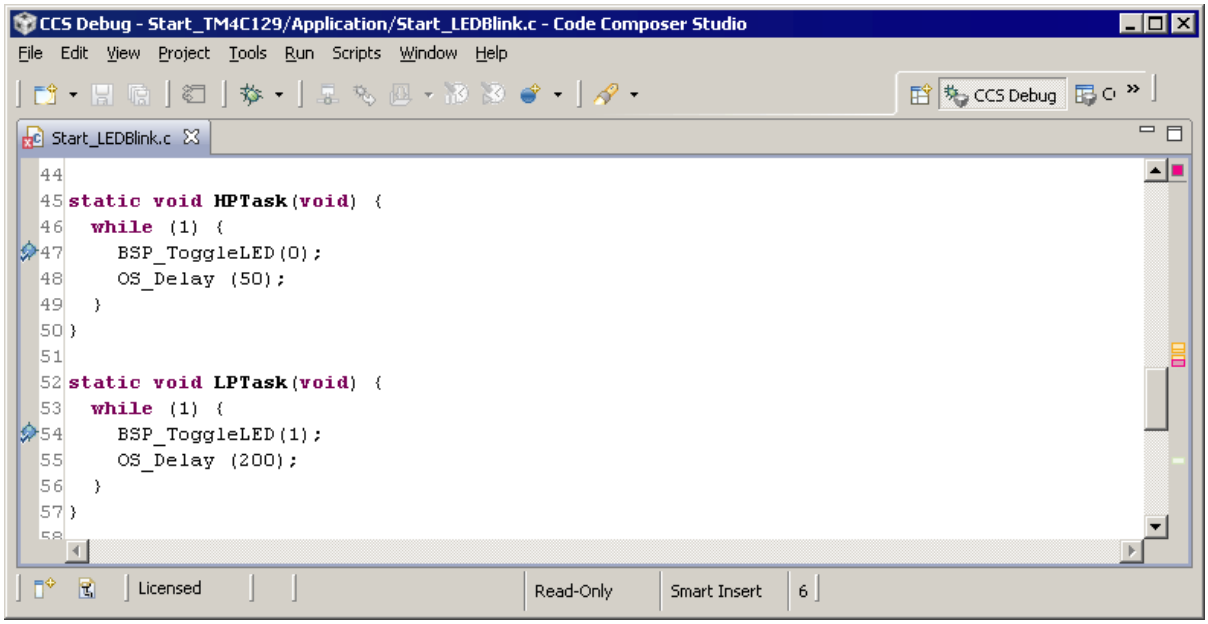
4.4 Stepping through the sample application

When starting the debugger, you will see the `main()` function (see example screenshot below). The `main()` function appears as long as project option **Run to main** is selected, which is enabled by default. Now you can step through the program. `OS_IncDI()` initially disables interrupts.
`OS_InitKern()` is part of the embOS library and written in assembler; you can therefore only step into it in disassembly mode. It initializes the relevant OS variables. Because of the previous call of `OS_IncDI()`, interrupts are not enabled during execution of `OS_InitKern()`.
`OS_InitHW()` is part of `RTOSInit_*.c` and therefore part of your application. Its primary purpose is to initialize the hardware required to generate the timer-tick-interrupt for embOS. Step through it to see what is done.

`OS_Start()` should be the last line in main, since it starts multitasking and does not return.

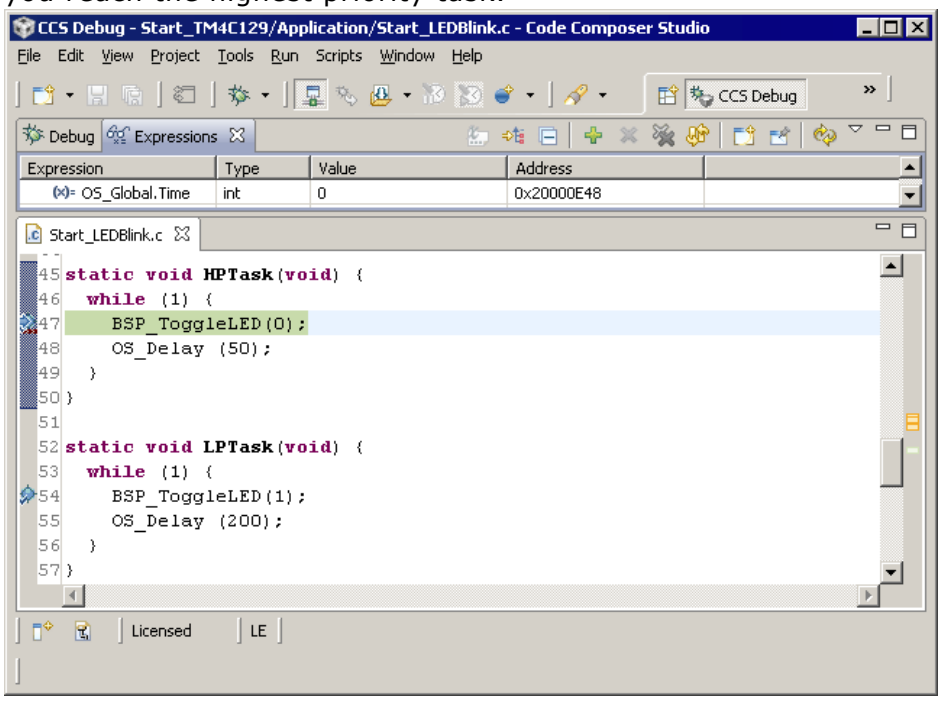


Before you continue stepping, you should set two break points in the two tasks as shown below:

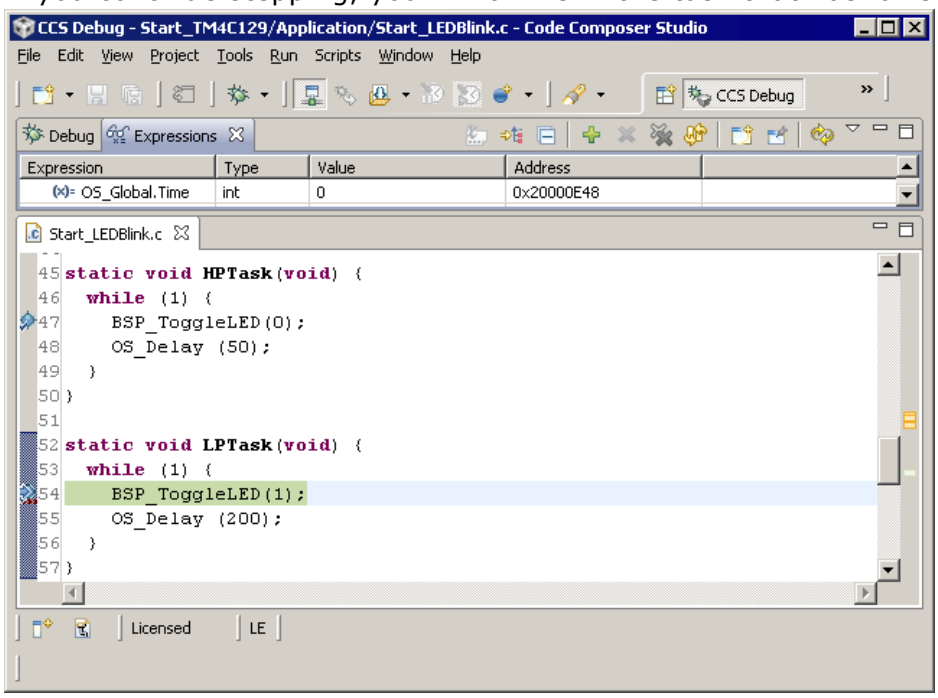


As `OS_Start()` is part of the embOS library, you can step through it in disassembly mode only. Y

Click **GO**, step over `OS_Start()`, or step into `OS_Start()` in disassembly mode until you reach the highest priority task.

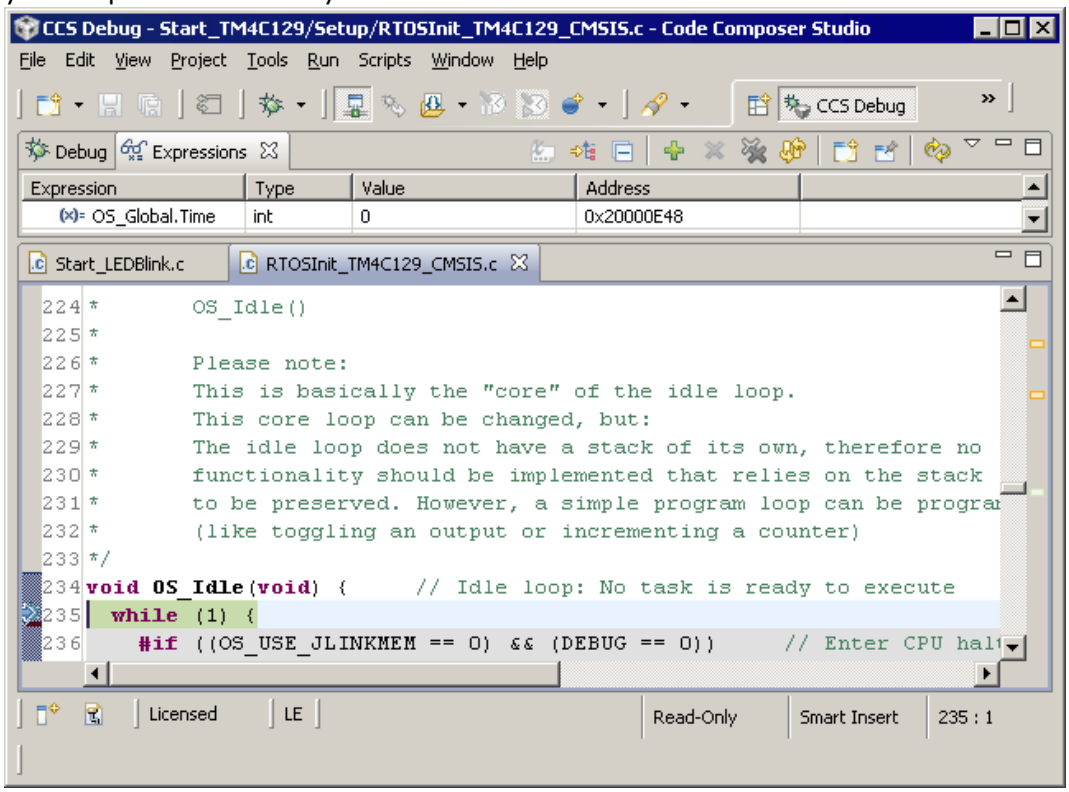


If you continue stepping, you will arrive in the task that has lower priority:



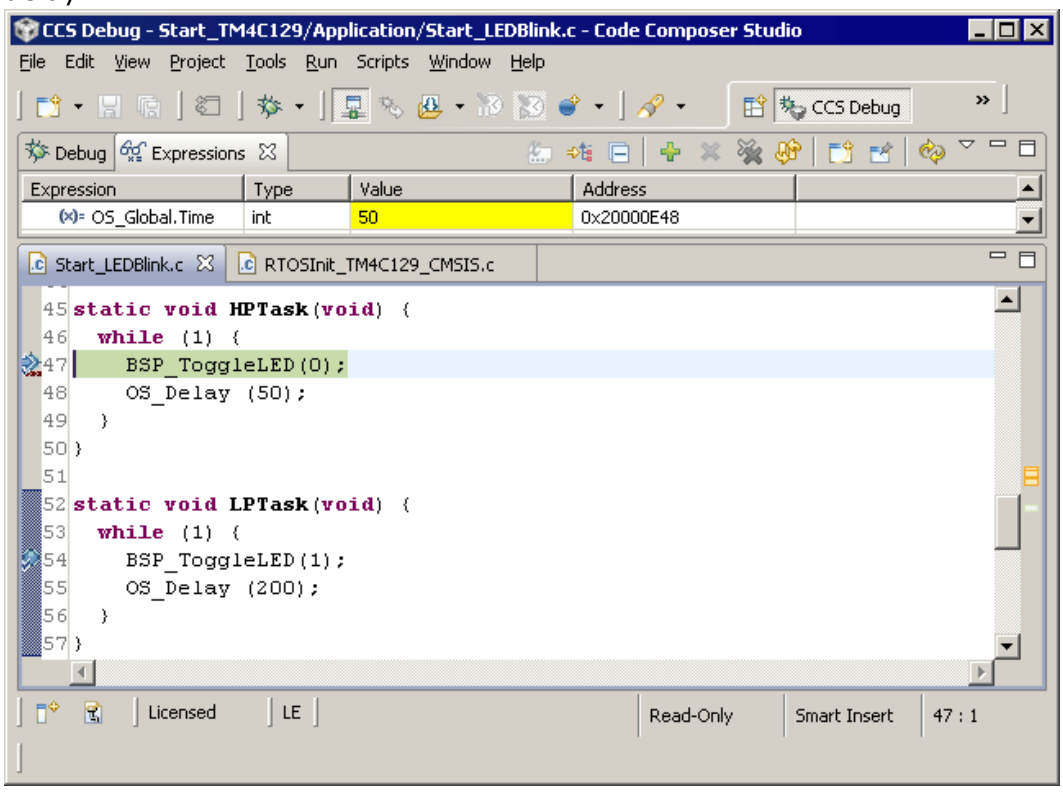
Continue to step through the program, there is no other task ready for execution. embOS will therefore start the idle-loop, which is an endless loop always executed if there is nothing else to do (no task is ready, no interrupt routine or timer executing).

You will arrive there when you step into the `OS_Delay()` function in disassembly mode. `OS_Idle()` is part of `RTOSInit*.c`.You may also set a breakpoint there before you step over the delay in `LPTask`.



If you set a breakpoint in one or both of our tasks, you will see that they continue execution after the given delay. Press GO to enter the highest priority task again.

As can be seen by the value of embOS timer variable OS_Global.Time, shown in the Watch window, `HPTask` continues operation after expiration of the 50 system tick delay.



Chapter 5

Build your own application

This chapter provides all information to setup your own embOS project.

5.1 Introduction

To build your own application, you should always start with one of the supplied sample workspaces and projects. Therefore, select an embOS workspace as described in First steps on page 9 and modify the project to fit your needs. Using a sample project as starting point has the advantage that all necessary files are included and all settings for the project are already done.

5.2 Required files for an embOS for Cortex M

To build an application using embOS, the following files from your embOS distribution are required and have to be included in your project:

- `RTOS.h` from subfolder `Inc\`.
  This header file declares all embOS API functions and data types and has to be included in any source file using embOS functions.
- RTOSInit_*.c from one target specific **BoardSupport\<Manufacturer>\<MCU>** subfolder.
  It contains hardware-dependent initialization code for embOS. It initializes the system timer interrupt and optional communication for embOSView via UART or JTAG.
- One embOS library from the subfolder **Lib**.
- OS_Error.c from one target specific subfolder **BoardSupport\<Manufacturer>\<MCU>**.The error handler is used if any debug library is used in your project.
- Additional CPU and compiler specific files may be required according to CPU.

When you decide to write your own startup code or use a low level init() function, ensure that non-initialized variables are initialized with zero, according to C standard. This is required for some embOS internal variables.
Your `main()` function has to initialize embOS by a call of `OS_InitKern()` and `OS_InitHW()` prior any other embOS functions are called.
You should then modify or replace the `OS_Start_LEDBlink.c` source file in the subfolder **Application**.

5.3 Change library mode

For your application you might want to choose another library. For debugging and program development you should use an embOS debug library. For your final application you may wish to use an embOS release library or a stack check library.

Therefore you have to select or replace the embOS library in your project or target:

- If your selected library is already available in your project, just select the appropriate configuration.
- To add a library, you may add the library to the existing Lib group. Exclude all other libraries from your build, delete unused libraries or remove them from the configuration.
- Check and set the appropriate `OS_LIBMODE_*` define as preprocessor option and/or modify the OS_Config.h file accordingly.

5.4 Select another CPU

embOS contains CPU-specific code for various Cortex M CPUs. Manufacturer- and CPU specific sample start workspaces and projects are located in the subfolders of the **BoardSupport** folder. To select a CPU which is already supported, just select the appropriate workspace from a CPU specific folder.

If your Cortex M CPU is currently not supported, examine all `RTOSInit` files in the CPU-specific subfolders and select one which almost fits your CPU. You may have to modify `OS_InitHW()`, `OS_COM_Init()`, the interrupt service routines for embOS system timer tick and communication to embOSView and the low level initialization.

Chapter 6

Libraries

This chapter describes the available embOS libraries.

6.1 CPU modes

embOS supports all memory and code model combinations that TICC / TI ARM compiler supports.

6.2 Naming conventions for prebuilt libraries

embOS for ARM Cortex-M and TI ARM compiler is shipped with different pre-built libraries with different combinations of the following features:

- Instruction set architecture - `Arch`
- CPU mode - `CpuMode`
- Byte order - `ByteOrder`
- FPU support - `FPU`
- Library mode - `LibMode`

The libraries are named as follows:

os<Arch>_<CpuMode>_<ByteOrder>_<FPU>_<LibMode>.a

Parameter	Meaning	Values
Arch	CPU Architecture	v7M4: Cortex M4F with VFP
CpuMode	Specifies the CPU mode	T: Always thumb
ByteOrder	Endianess	be: Big endian le: Little endian
FPU	FPU support	v4SPD16: VFPv4SPD16
LibMode	Library mode	XR: eXtreme Release R: Release S: Stack check D: Debug SP: Stack check + Profiling DP: Debug + Profiling DT: Debug + Trace

Example:

osv7M4_T_le_v4SPD16_DP.lib is the library for a project using a CortexM4F with VFP, thumb mode, little endian mode with debug and profiling support.

Chapter 7

CPU and Compiler specifics

7.1 Standard system libraries

embOS for Cortex-M and TI ARM compiler may be used with standard TI ARM system libraries for most of all projects. Heap management and file operation functions of standard system libraries are not reentrant and can therefore not be used with embOS, if non thread safe functions are used from different tasks. For heap management, embOS delivers its own thread safe functions which may be used. These functions are described in embOS CPU independent manual.

7.2 Reentrancy, thread safe management

Using embOS with C++ projects and file operations or just normal call of heap management functions may require thread-safe system libraries if these functions are called from different tasks. Thread-safe system libraries require some locking mechanism which is RTOS specific.

To switch the system libraries to thread safe mode, the embOS function OS_InitSysLocks() which is includeds in the embOS libraries has to be called before the system is started. A typical embOS initialization for thread safe usage of system libraries with TI ARM compiler would look like follows:

```
int main(void) {
  OS_IncDI();                      /* Initially disable interrupts  */
  OS_InitKern();                   /* Initialize OS                 */
  OS_InitSysLocks();               /* Activate thread safe library  */
  OS_InitHW();                     /* Initialize Hardware for OS    */
  /* You need to create at least one task before calling OS_Start() */
  OS_CREATETASK(&TCBHP, "HP Task", HPTask, 100, StackHP);
  OS_CREATETASK(&TCBLP, "LP Task", LPTask,  50, StackLP);
  OS_Start();                      /* Start multitasking            */
  return 0;
}
```


Chapter 8

Stacks

This chapter describes how embOS uses the different stacks of the Cortex M CPU.

8.1 Task stack for Cortex-M

Each task uses its individual stack. The stack pointer is initialized and set every time a task is activated by the scheduler. The stack-size required for a task is the sum of the stack-size of all routines, plus a basic stack size, plus size used by exceptions.

The basic stack size is the size of memory required to store the registers of the CPU plus the stack size required by calling embOS-routines.

For the Cortex M CPUs, this minimum basic task stack size is about 72 bytes. Because any function call uses some amount of stack and every exception also pushes at least 32 bytes onto the current stack, the task stack size has to be large enough to handle one exception too. We recommend at least 256 bytes stack as a start.

8.2 System stack for Cortex-M

The embOS system executes in thread mode, the scheduler executes in handler mode. The minimum system stack size required by embOS is about 136 bytes (stack check & profiling build). However, since the system stack is also used by the application before the start of multitasking (the call to OS_Start()), and because software-timers and C-level interrupt handlers also use the system-stack, the actual stack requirements depend on the application.

The size of the system stack can be changed in the project settings.

8.3 Interrupt stack for Cortex-M

If a normal hardware exception occurs, the Cortex-M core switches to handler mode mode, which uses the main stack pointer. With embOS, the main stack pointer is initialized to use the system-stack which is defined in the project settings. A separate irq-stack is not used, interrupts run on the system stack. The main stack is also used as stack by the embOS scheduler and during idle times, when no task is ready to run and OS_Idle() is executed.

Chapter 9

Interrupts

The Cortex M core comes with an built-in vectored interrupt controller which supports up to 32 separate interrupt sources. The real number of interrupt sources depends on the specific target CPU.

9.1 What happens when an interrupt occurs?

- The CPU-core receives an interrupt request from the interrupt controller.
- As soon as the interrupts are enabled, the interrupt is accepted and executed.
- The CPU pushes temporary registers and the return address onto the current stack.
- The CPU switches to handler mode and main stack.
- The CPU saves an exception return code and current flags onto the main stack.
- The CPU jumps to the vector address delivered by the NVIC.
- The interrupt handler is processed.
- The interrupt handler ends with a return from interrupt. by reading the exception return code.
- The CPU switches back to the mode and stack which was active before the exception was called.
- The CPU restores the temporary registers and return address from the stack and continues the interrupted function.

9.2 Defining interrupt handlers in C

Interrupt handlers for Cortex M cores are written as normal C-functions which do not take parameters and do not return any value. Interrupt handler which call an embOS function need a prolog and epilog function as described in the generic manual and in the examples below.

Example

Simple interrupt routine:

```
static void _Systick(void) {
  OS_EnterNestableInterrupt(); // Inform embOS that interrupt code is running
  OS_HandleTick();             // May be interrupted by higher priority interrupts
  OS_LeaveNestableInterrupt(); // Inform embOS that interrupt handler is left
}
```

9.3 Interrupt vector table

After Reset, the ARM Cortex M CPU uses an initial interrupt vector table which is located in ROM at address 0x00. It contains the address for the main stack and addresses for all exceptions handlers.

The interrupt vector table is located in a C source or assembly file in the CPU specific subfolder. All interrupt handler function addresses have to be inserted in the vector table, as long as a RAM vector table is not used.

The vector table may be copied to RAM to enable variable interrupt handler installation. The compile time switch OS_USE_VARINTTABLE is used to enable usage of a vector table in RAM.

To save RAM, the switch is set to zero per default in RTOSInit_*.c. It may be overwritten by project settings to enable the vector table in RAM. The first call of OS_InstallISRHandler() will then automatically copy the vector table into RAM. When using your own interrupt vector table, ensure that the addresses of the embOS exception handlers OS_Exception() and OS_Systick() are included.
When the vector table is not located at address 0x00, the vector base register in the NVIC controller has to be initialized to point to the vector table base address.

9.4 Interrupt-stack switching

Since Cortex M core based controllers have two separate stack pointers, and embOS runs the user application on the process stack, there is no need for explicit stack-switching in an interrupt routine which runs on the main stack. The routines OS_EnterIntStack() and OS_LeaveIntStack() are supplied for source code compatibility to other processors only and have no functionality.

9.5 Zero latency interrupts

9.5.1 Zero latency interrupts with Cortex M

Instead of disabling interrupts when embOS does atomic operations, the interrupt level of the CPU is set to 128. Therefore all interrupt priorities higher than 128 can still be processed. Please note that lower priority numbers define a higher priority. All interrupts with priority level from 0 to 127 are never disabled. These interrupts are named fast interrupts. You must not execute any embOS function from within a fast interrupt function.

9.6 Interrupt priorities

This chapter describes interrupt priorities supported by the Cortex M core.
The priority is any number between 0 and 255 as seen by the CPU core. With embOS and its own setup functions for the interrupt controller and priorities, there is no difference in the priority values regardless of the different preemption level of specific devices.
Using the CMSIS functions to set up interrupt priorities requires different values for the priorities. These values depend on the number of preemtion levels of the specific chip. a description is found in the chapter CMSIS.

9.6.1 Interrupt priorities with Cortex M cores

The Cortex M3 support up to 256 levels of programmable priority with a maximum of 128 levels of preemption. Most Cortex M chips have fewer supported levels, for example 8, 16, 32, and so on. The chip designer can customize the chip to obtain the levels required. There is a minimum of 8 preemption levels. Every interrupt with a higher preemption level may preempt any other interrupt handler running on a lower preemption level. Interrupts with equal preemption level may not preempt each other.

With introduction of Fast interrupts, interrupt priorities useable for interrupts using embOS API functions are limited.

- Any interrupt handler using embOS API functions has to run with interrupt priorities from 128 to 255. These embOS interrupt handlers have to start with `OS_EnterInterrupt()` or `OS_EnterNestableInterrupt()` and have to end with `OS_LeaveInterrupt()` or `OS_LeaveNestableInterrupt()`.
- Any Fast interrupt (running at priorities from 0 to 127) must not call any embOS API function. Even `OS_EnterInterrupt()` and `OS_LeaveInterrupt()` must not be called.
- Interrupt handlers running at low priorities (from 128 to 255) not calling any embOS API function are allowed, but must not reenable interrupts! The priority limit between embOS interrupts and Fast interrupts is fixed to 128 and can only be changed by recompiling embOS libraries! This is done for efficiency reasons. Basically the define `OS_IPL_DI_DEFAULT` in RTOS.h and the RTOS.s file must be modified. There might be other modifications necessary. Please contact the embOS support if you like to change this threshold.

9.6.2 Priority of the embOS scheduler

The embOS scheduler runs on the lowest interrupt priority. The scheduler may be preempted by any other interrupt with higher preemption priority level. The application interrupts shall run on higher preemption levels to ensure short reaction time.

During initialization, the priority of the embOS scheduler is set to 0x03 for Cortex M0 and to 0xFF for Cortex M3 / M4 and M4F, which is the lowest preemption priority regardless of the number of preemption levels.

9.6.3 Priority of the embOS system timer

The embOS system timer runs on the second lowest preemption level. Thus, the embOS timer may preempt the scheduler. Application interrupts which require fast reaction should run on a higher preemption priority level.

9.6.4 Priority of embOS software timers

The embOS software timer callback functions are called from the scheduler and run on the schedulers preemption priority level which is the lowest interrupt priority level. To ensure short reaction time of other interrupts, other interrupts should run on a higher preemption priority level and the software timer callback functions should be as short as possible.

9.6.5 Priority of application interrupts for Cortex M3 core

Application interrupts using embOS functions may run on any priority level between 255 to 128. However, interrupts which require fast reaction should run on higher priority levels than the embOS scheduler and the embOS system timer to allow preemption of theses interrupt handlers. Interrupt handlers which require fast reaction may run on higher priorities than 128, but must not call any embOS function (fast interrupts). We recommend that application interrupts should run on a higher preemption level than the embOS scheduler, at least at the second lowest preemption priority level.

As the number of preemption levels is chip specific, the second lowest preemption priority varies depending on the chip. If the number of preemption levels is not documented, the second lowest preemption priority can be set as follows, using embOS functions:

```
unsigned char Priority;
OS_ARM_ISRSetPrio(_ISR_ID, 0xFF);              // Set to lowest level, ALL BITS set
Priority  = OS_ARM_ISRSetPrio(_ID_TICK, 0xFF); // Read priority back
Priority -= 1;                                 // Lower preemption level
OS_ARM_ISRSetPrio(_ISR_ID, Priority);
```

9.7 Interrupt nesting

The Cortex M CPU uses a priority controlled interrupt scheduling which allows nesting of interrupts per default. Any interrupt or exception with a higher preemption priority may interrupt an interrupt handler running on a lower preemption priority. An interrupt handler calling embOS functions has to start with an embOS prolog function; it informs embOS that an interrupt handler is running. For any interrupt handler, the user may decide individually whether this interrupt handler may be preempted or not by choosing the prolog function.

9.7.1 OS_EnterInterrupt()

Description

`OS_EnterInterrupt()` disables nesting

Prototype

```
void OS_EnterInterrupt(void)
```

Return value

None.

Additional Information

`OS_EnterInterrupt()` has to be used as prolog function, when the interrupt handler should not be preempted by any other interrupt handler that runs on a priority below the fast interrupt priority. An interrupt handler that starts with `OS_EnterInterrupt()` has to end with the epilog function `OS_LeaveInterrupt()`.

Example

Interrupt-routine that can not be preempted by other interrupts.

```
static void _Systick(void) {
  OS_EnterInterrupt();  // Inform embOS that interrupt code is running
  OS_HandleTick();      // Can not be interrupted by higher priority interrupts
  OS_LeaveInterrupt();  // Inform embOS that interrupt handler is left
}
```

9.7.2 OS_EnterNestableInterrupt()

Description

`OS_EnterNestableInterrupt()` enables nesting.

Prototype

```
void OS_EnterNestableInterrupt(void)
```

Return value

None.

Additional Information

`OS_EnterNestableInterrupt()`, allow nesting. `OS_EnterNestableInterrupt()` may be used as prolog function, when the interrupt handler may be preempted by any other interrupt handler that runs on a higher interrupt priority. An interrupt handler that starts with `OS_EnterNestableInterrupt()` has to end with the epilog function `OS_LeaveNestableInterrupt()`.

Example

Interrupt-routine that can be preempted by other interrupts.

```
static void _Systick(void) {
  OS_EnterNestableInterrupt();  // Inform embOS that interrupt code is running
  OS_HandleTick();              // Can be interrupted by higher priority interrupts
  OS_LeaveNestableInterrupt();  // Inform embOS that interrupt handler is left
}
```

9.7.3 Required embOS system interrupt handler

embOS for Cortex M core needs two exception handlers which belong to the system itself. Both are delivered with embOS. Ensure that they are referenced in the vector table.

9.8 Interrupt handling with vectored interrupt controller

For the Cortex M core, which has a built-in vectored interrupt controller, embOS delivers additional functions to install and setup interrupt handler functions. To handle interrupts with the vectored interrupt controller, embOS offers the following functions:

9.8.1 OS_ARM_EnableISR(): Enable specific interrupt

Description

`OS_ARM_EnableISR()` is used to enable interrupt acceptance of a specific interrupt source in a vectored interrupt controller.

Prototype

```
void OS_ARM_EnableISR(int ISRIndex)
```

Parameter	Description
ISRIndex	Index of the interrupt source which should be enabled. Note that the index counts from 0 for the first entry in the vector table.

Return value

None.

Additional Information

This function just enables the interrupt inside the interrupt controller. It does not enable the interrupt of any peripherals. This has to be done elsewhere.
Note that the ISRIndex counts from 0 for the first entry in the vector table.
The first peripheral index therefore has the ISRIndex 16, because the first peripheral interrupt vector is located after the 16 generic vectors in the vector table.
This differs from index values used with CMSIS.

9.8.2 OS_ARM_DisableISR(): Disable specific interrupt

Description

`OS_ARM_DisableISR()` is used to disable interrupt acceptance of a specific interrupt source in a vectored interrupt controller which is not of the VIC type.

Prototype

```
void OS_ARM_DisableISR(int ISRIndex)
```

Parameter	Description
ISRIndex	Index of the interrupt source which should be disabled. Note that the index counts from 0 for the first entry in the vector table.

Return value

None.

Additional Information

This function just disables the interrupt in the interrupt controller. It does not disable the interrupt of any peripherals. This has to be done elsewhere.
Note that the ISRIndex counts from 0 for the first entry in the vector table.

The first peripheral index therefore has the ISRIndex 16, because the first peripheral interrupt vector is located after the 16 generic vectors in the vector table.
This differs from index values used with CMSIS.

9.8.3 OS_ARM_ISRSetPrio(): Set priority of specific interrupt

Description

`OS_ARM_ISRSetPrio()` is used to set or modify the priority of a specific interrupt source by programming the interrupt controller.

Prototype

```
int OS_ARM_ISRSetPrio(int ISRIndex, int Prio);
```

Parameter	Description
`ISRIndex`	Index of the interrupt source which should be modified. Note that the index counts from 0 for the first entry in the vector table.
`Prio`	The priority which should be set for the specific interrupt. Prio ranges from 0 (highest priority) to 255 (lowest priority).

Return value

None.

Additional Information

This function sets the priority of an interrupt channel by programming the interrupt-controller. Please refer to CPU-specific manuals about allowed priority levels.
Note that the ISRIndex counts from 0 for the first entry in the vector table.
The first peripheral index therefore has the ISRIndex 16, because the first peripheral interrupt vector is located after the 16 generic vectors in the vector table.
This differs from index values used with CMSIS.
The priority value is independent of the chip-specific preemption levels. Any value between 0 and 255 can be used, were 255 always is the lowest priority and 0 is the highest priority.
The function can be called to set the priority for all interrupt sources, regardless of whether embOS is used or not in the specified interrupt handler.
Note that interrupt handlers running on priorities from 127 or higher must not call any embOS function.

Chapter 10

VFP support

10.1 Vector Floating Point support VFPv4

Some Cortex M4 / M4F MCUs come with an integrated vectored floating point unit VFPv4.
When selecting the CPU and activating the VFPv4 support in the project options, the compiler and linker will add efficient code which uses the VFP when floating point operations are used in the application.
With embOS, the VFP registers are automatically saved and restored when preemptive or cooperative task switches are performed.
For efficiency reasons, embOS does not save and restore the VFP registers for tasks which do not use the VFP unit.

10.1.1 Using embOS libraries with VFP support

When VFP support is selected as project option, one of the embOS libraries with VFP support have to be used in the project.
The embOS libraries for VFP support require that the VFP is switched on during startup and remains switched on during program execution.
Using your own startup code, ensure that the VFP is switched on during startup.
When the VFP unit is not switched on, the embOS scheduler will fail.
The debug version of embOS checks whether the VFP is switched on when embOS is initialized by calling `OS_InitKern()`.
When the VFP unit is not detected or not switched on, the embOS error handler `OS_Error()` is called with error code `OS_ERR_CPU_STATE_ILLEGAL`.

10.1.2 Using the VFP in interrupt service routines

Using the VFP in interrupt service routines does not require any additional functions to save and restore the VFP registers. The VFP registers are automatically saved and restored by the hardware.

Chapter 11

RTT and SystemView

This chapter contains information about SEGGER Real Time Transfer and SEGGER SystemView.

11.1 SEGGER Real Time Transfer

SEGGER's Real Time Transfer (RTT) is the new technology for interactive user I/O in embedded applications. RTT can be used with any J-Link model and any supported target processor which allows background memory access.

RTT is included with many embOS start projects. These projects are by default configured to use RTT for debug output.
Some IDEs, such as SEGGER Embedded Studio, support RTT and display RTT output directly within the IDE. In case the used IDE does not support RTT, SEGGER's J-Link RTT Viewer, J-Link RTT Client, and J-Link RTT Logger may be used instead to visualize your application's debug output.

For more information on SEGGER Real Time Transfer, refer to https://www.segger.com/jlink-rtt.html.

11.1.1 Shipped files related to SEGGER RTT

All files related to SEGGER RTT are shipped inside the respective start project's `Setup` folder:

File	Description
SEGGER_RTT.c	Generic implementation of SEGGER RTT.
SEGGER_RTT.h	Generic implementation header file.
SEGGER_RTT_Conf.h	Generic RTT configuration file.
SEGGER_RTT_printf.c	Generic printf() replacement to write formatted data via RTT.
SEGGER_RTT_Syscalls_*.c	Compiler-specific low-level functions for using printf() via RTT. If this file is included in a project, RTT is used for debug output. To use the standard out of your IDE, exclude this file from build.

11.2 SEGGER SystemView

SEGGER SystemView is a real-time recording and visualization tool to gain a deep understanding of the runtime behavior of an application, going far beyond what debuggers are offering. The SystemView module collects and formats the monitor data and passes it to RTT.

SystemView is included with many embOS start projects. These projects are by default configured to use SystemView in debug builds. The associated PC visualization application, SystemViewer, is not shipped with embOS. Instead, the most recent version of that application is available for download from our website.

For more information on SEGGER SystemView, including the SystemViewer download, refer to https://www.segger.com/systemview.html.

11.2.1 Shipped files related to SEGGER SystemView

All files related to SEGGER SystemView are shipped inside the respective start project's `Setup` folder:

File	Description
Global.h	Global type definitios required by SEGGER SystemView.
SEGGER.h	Generic types and utility function header.
SEGGER_SYSVIEW.c	Generic implementation of SEGGER RTT.
SEGGER_SYSVIEW.h	Generic implementation include file.
SEGGER_SYSVIEW_Conf.h	Generic configuration file.
SEGGER_SYSVIEW_ConfDefaults.h	Generic default configuration file.
SEGGER_SYSVIEW_Config_embOS.c	Target-specific configuration of SystemView with embOS.
SEGGER_SYSVIEW_embOS.c	Generic interface implementation for SystemView with embOS.
SEGGER_SYSVIEW_embOS.h	Generic interface implementation header file for SystemView with embOS.
SEGGER_SYSVIEW_Int.h	Generic internal header file.

Chapter 12

Technical data

12.1 Memory requirements

These values are neither precise nor guaranteed, but they give you a good idea of the memory-requirements. They vary depending on the current version of embOS. The kernel itself has a minimum ROM size requirement of about 1.700 bytes.

In the table below, which is for X-Release build, you can find minimum RAM size requirements for embOS resources. Note that the sizes depend on selected embOS library mode.

embOS resource	RAM [bytes]
Task control block	32
Resource semaphore	16
Counting semaphore	8
Mailbox	24
Software timer	20

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