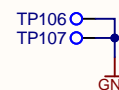

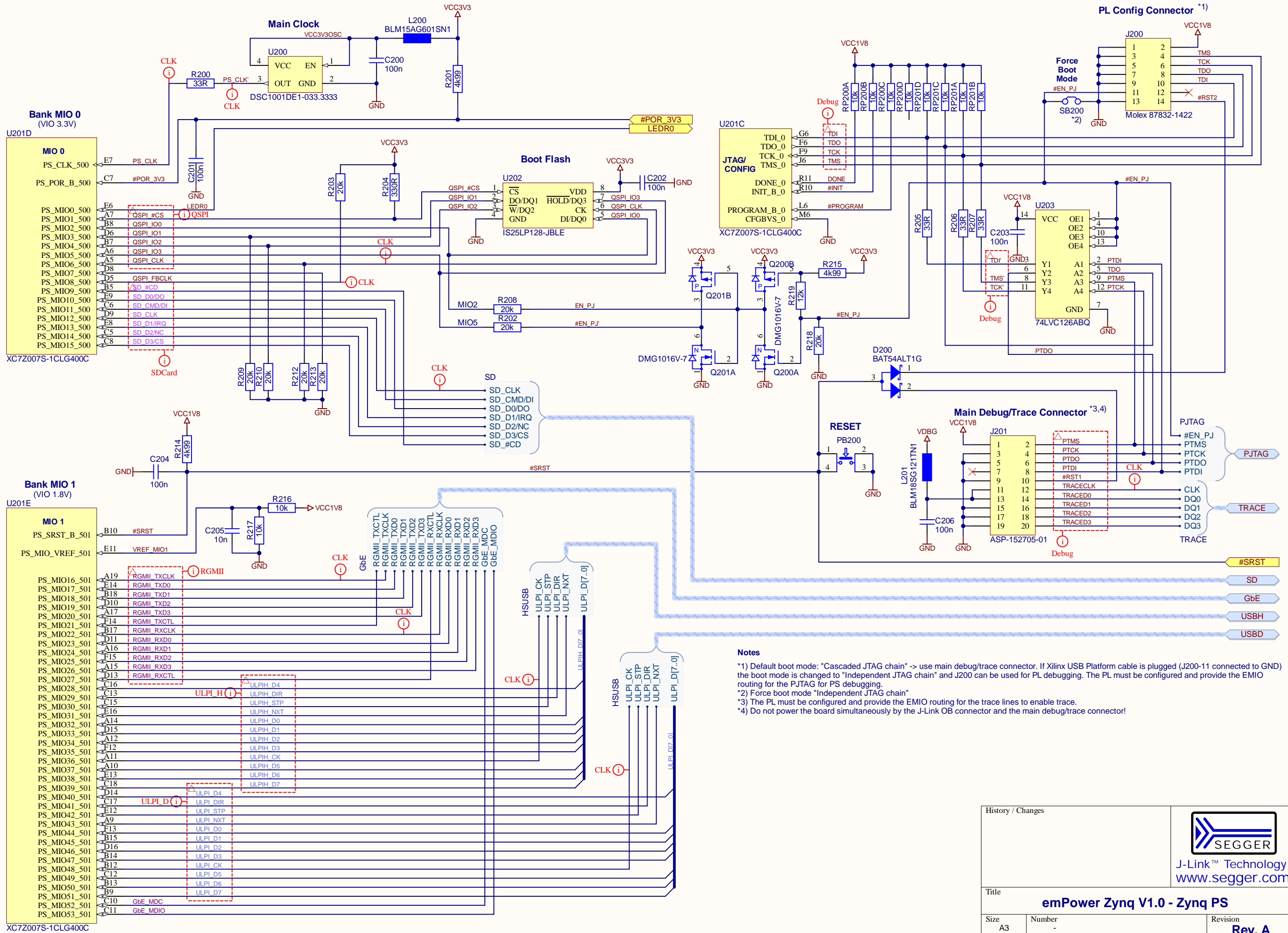


Notes

-
- Unless specified otherwise:
 - Ceramic capacitors are of type X5R/X7R or C0G/NP0 with a voltage rating of at least 6.3V (100n at least 16V)
 - Resistors are 1% tolerance types




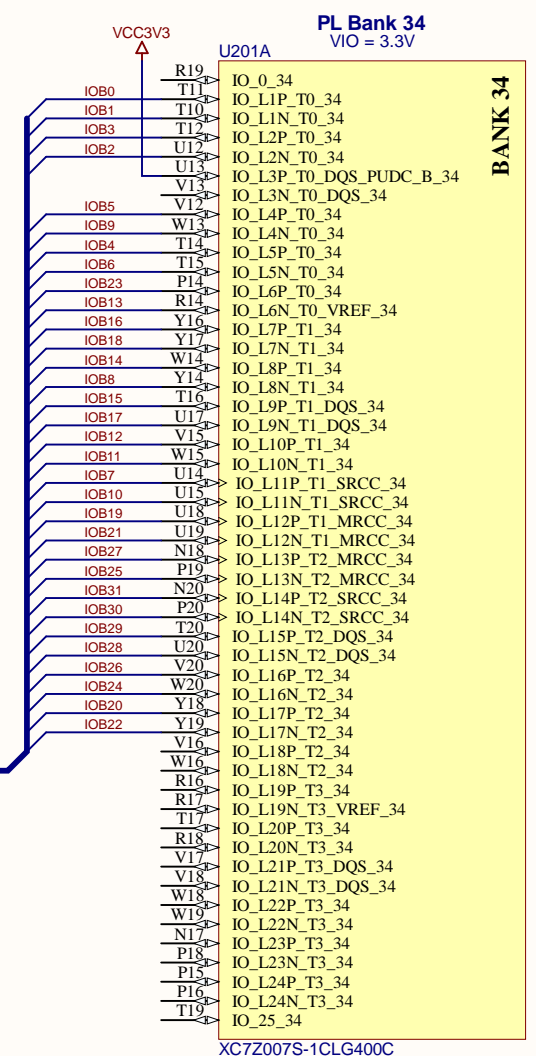
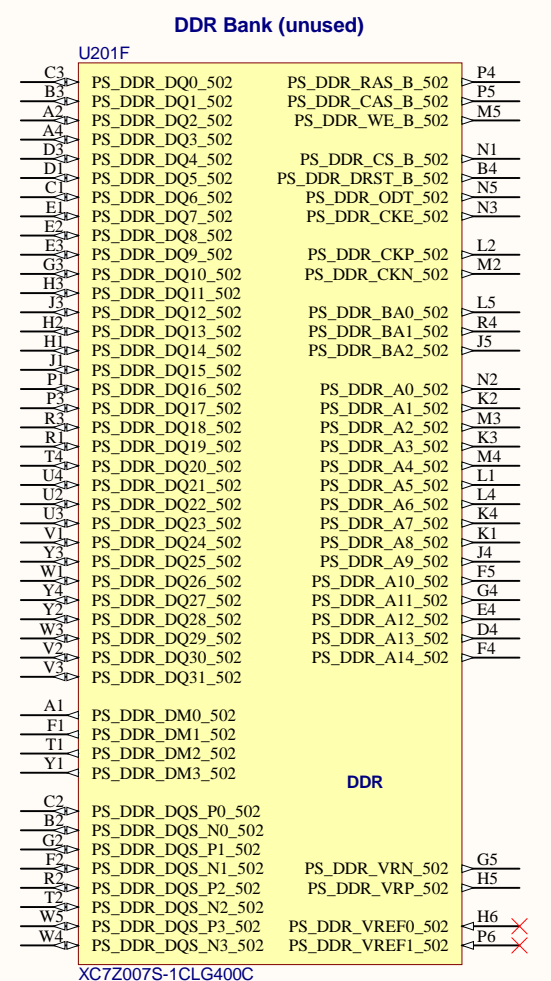
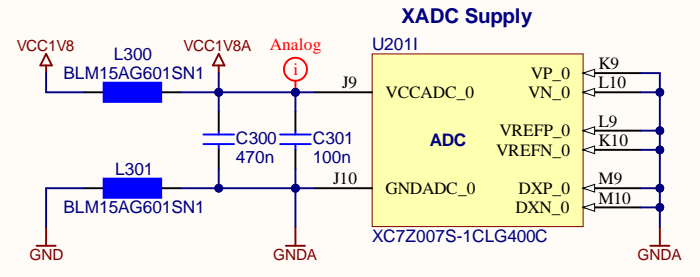
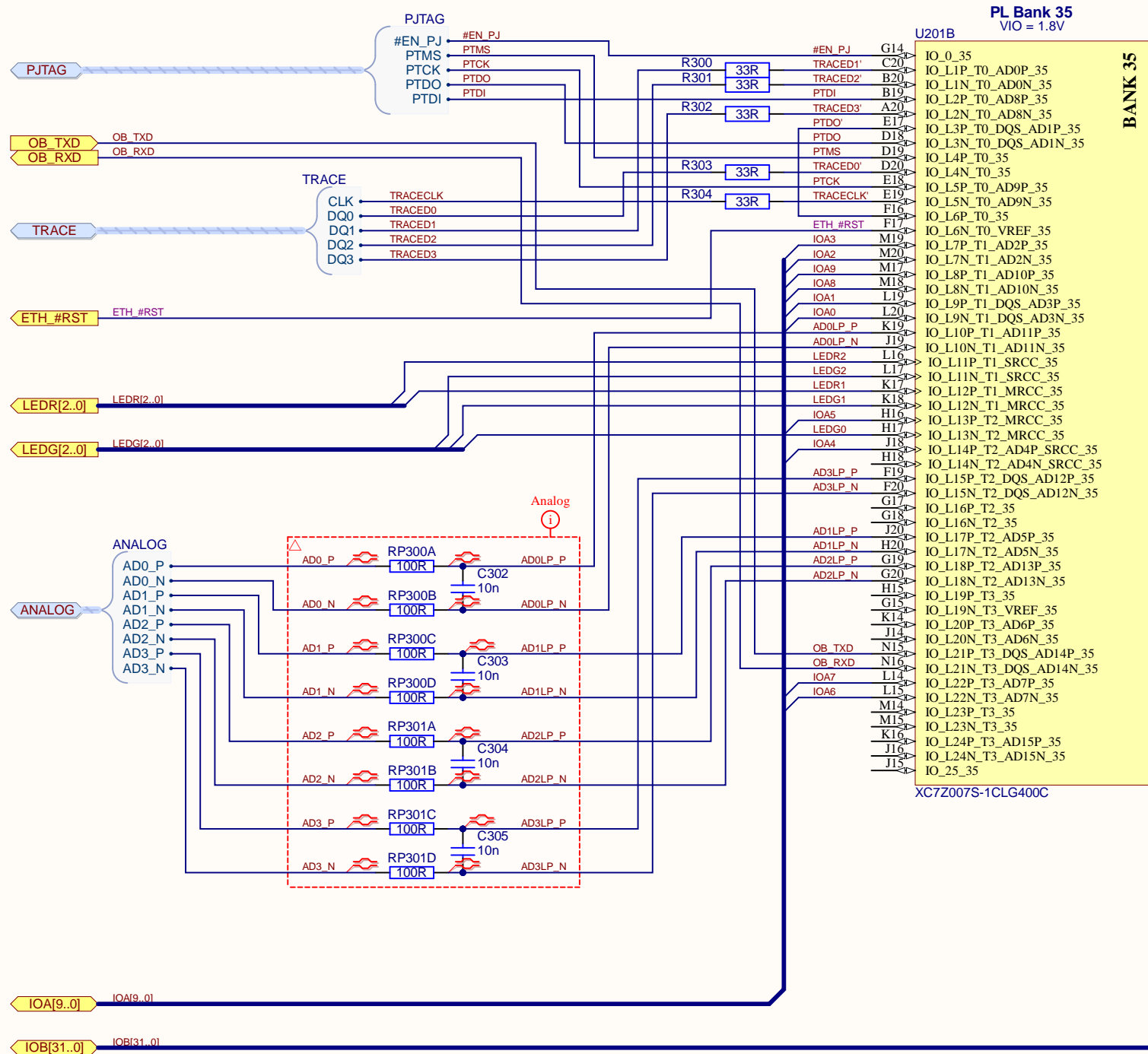
History / Changes		 J-Link™ Technology www.segger.com
Title		
emPower Zynq V1.0 - Top Level		
Size	Number	Revision
A3	-	Rev. A
Date:	190702	Sheet 1 / 7
File:	Sheet01_TopLevel_WEB.SchDoc	Drawn: VK



Notes

- *1) Default boot mode: "Cascaded JTAG chain" -> use main debug/trace connector. If Xilinx USB Platform cable is plugged (J200-11 connected to GND) the boot mode is changed to "Independent JTAG chain" and J200 can be used for PL debugging. The PL must be configured and provide the EMIO routing for the PJTAG for PS debugging.
- *2) Force boot mode "Independent JTAG chain"
- *3) The PL must be configured and provide the EMIO routing for the trace lines to enable trace.
- *4) Do not power the board simultaneously by the J-Link OB connector and the main debug/trace connector!

History / Changes		 J-Link™ Technology www.segger.com			
Title				emPower Zynq V1.0 - Zynq PS	
Size	A3	Number	-	Revision	Rev. A
Date:	190702	Sheet	2 / 7		
File:	Sheet02_ZynqPS_WEB.SchDoc	Drawn:	VK		



History / Changes

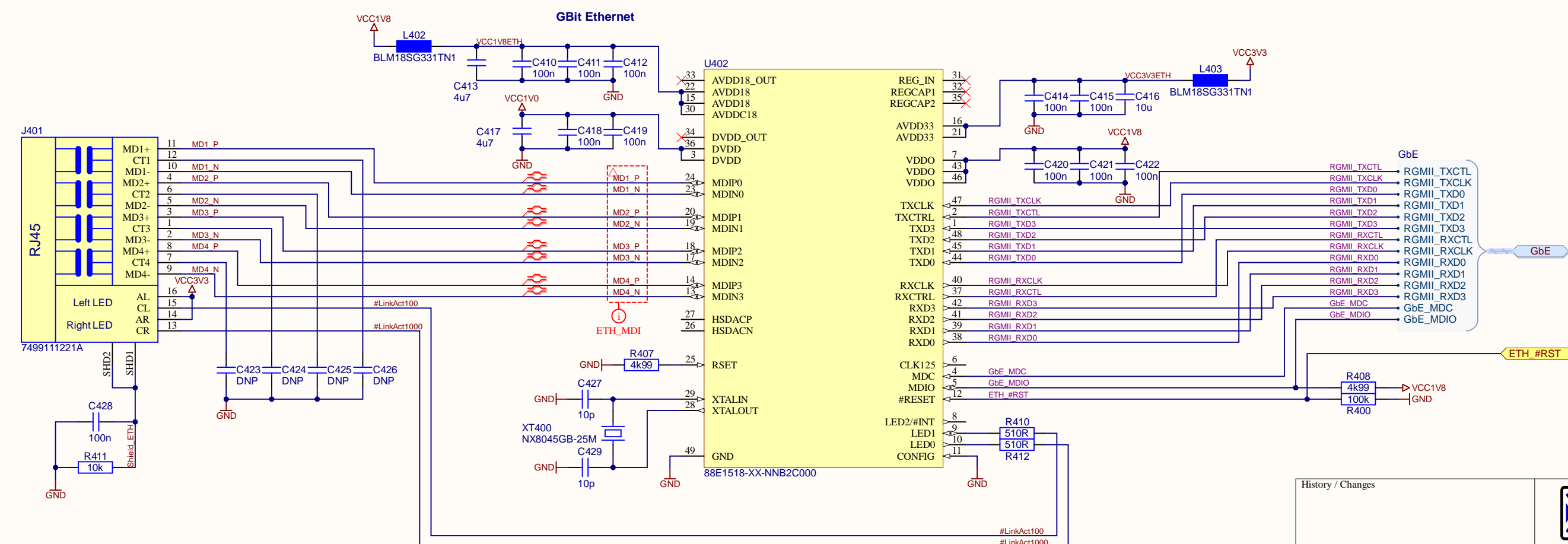
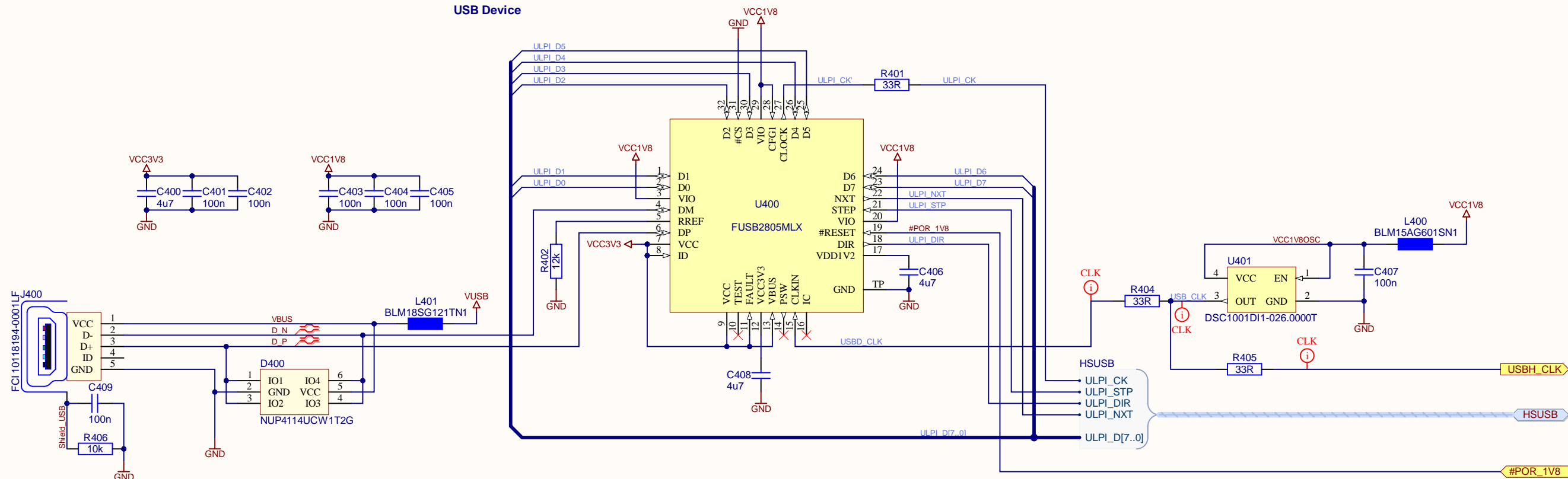
J-Link™ Technology
www.segger.com


Title
emPower Zynq V1.0 - Zynq PL

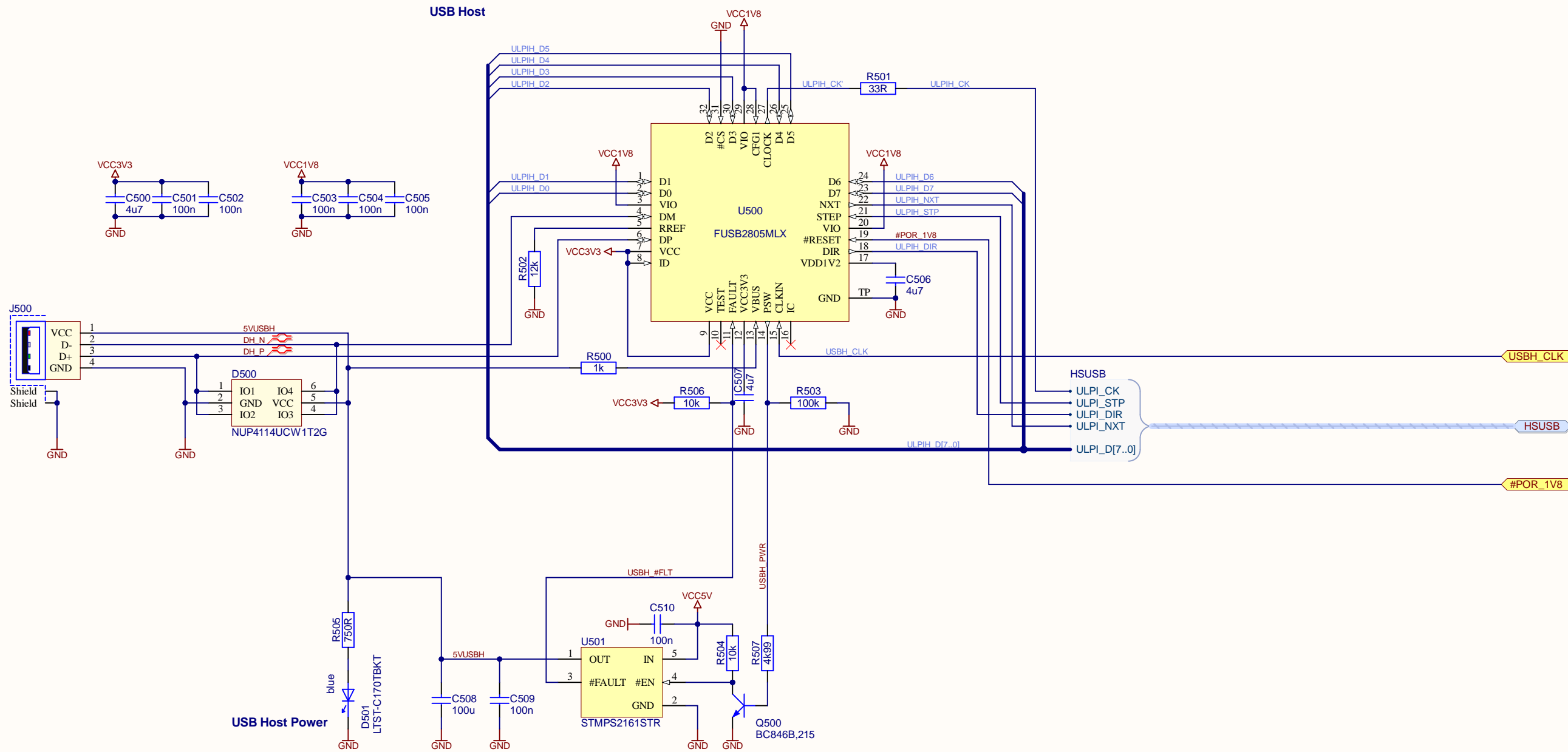
Size A3	Number -	Revision Rev. A
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Date: 190702
File: Sheet03_ZynqPL_WEB.SchDoc

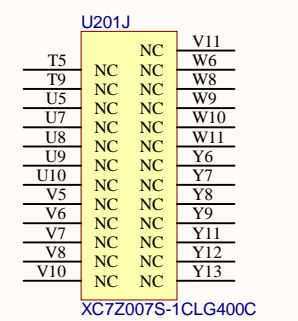
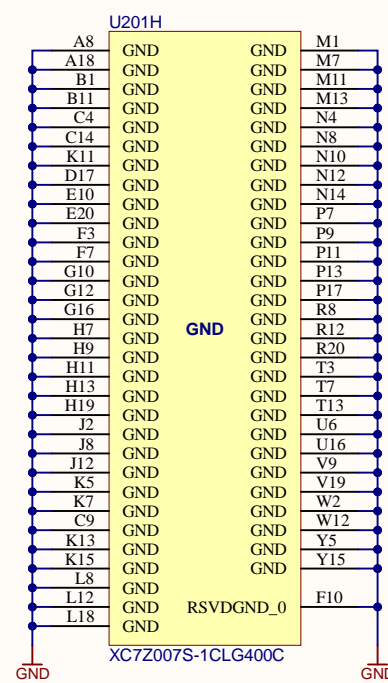
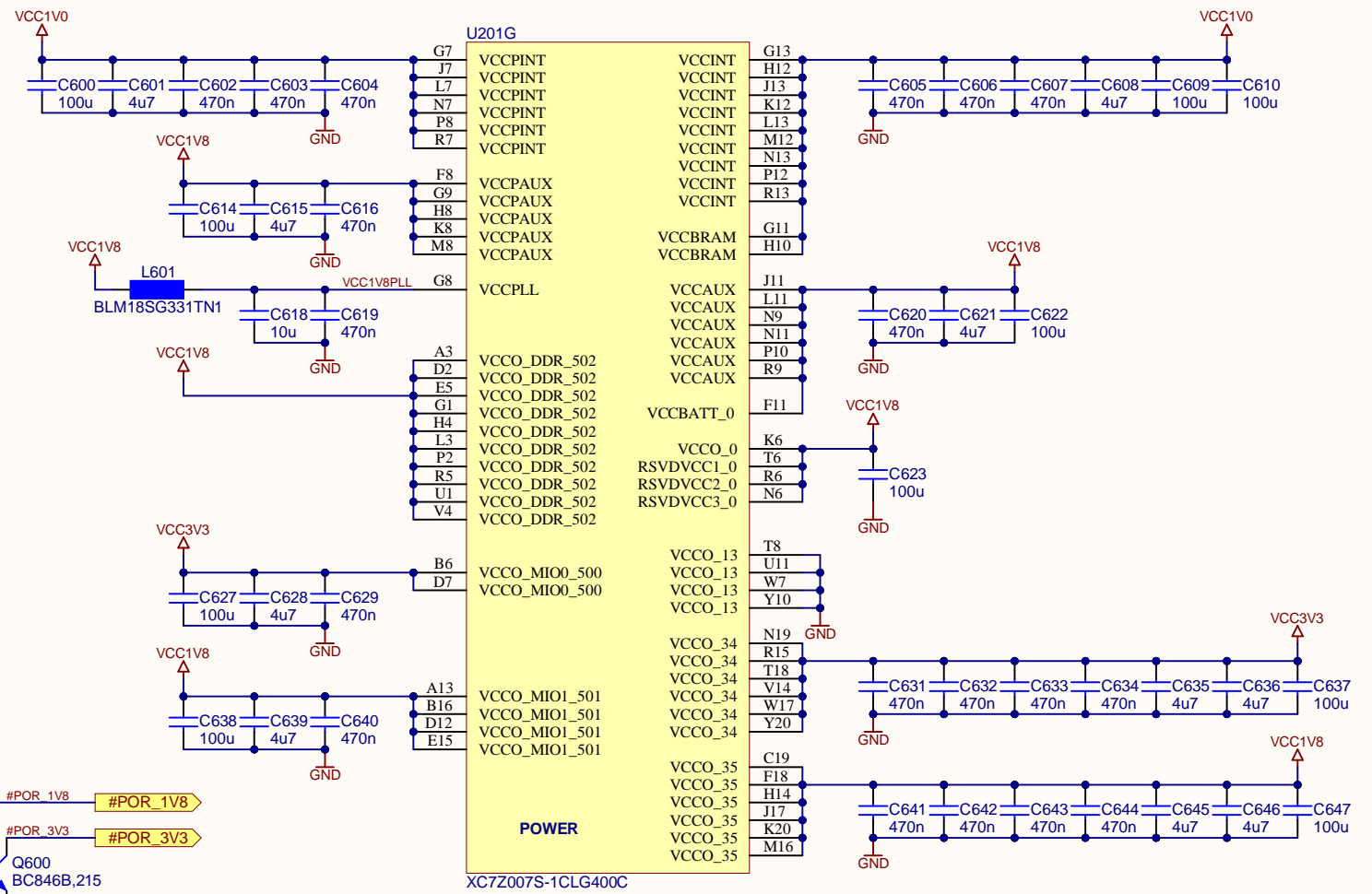
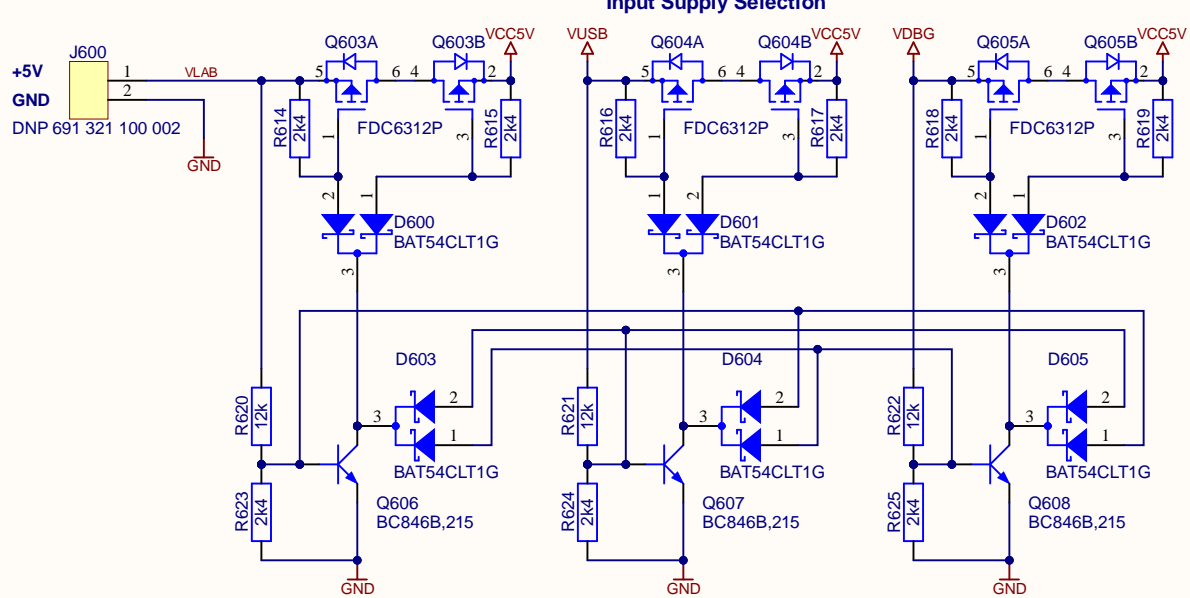
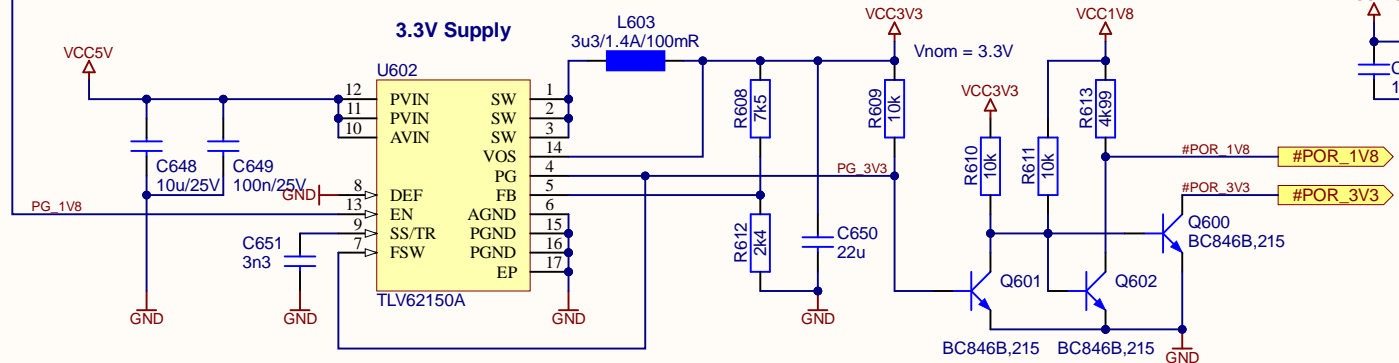
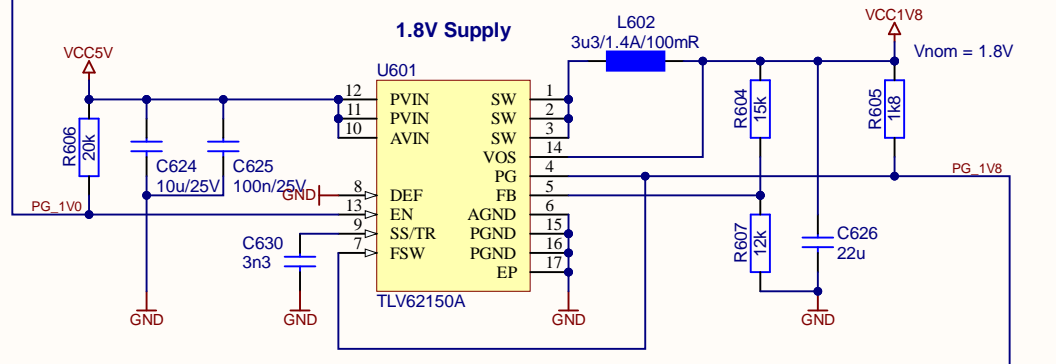
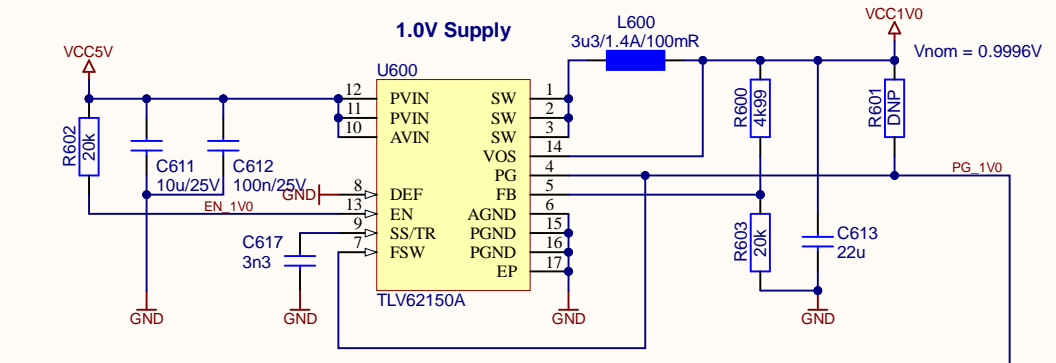
Sheet 3 / 7
Drawn: VK




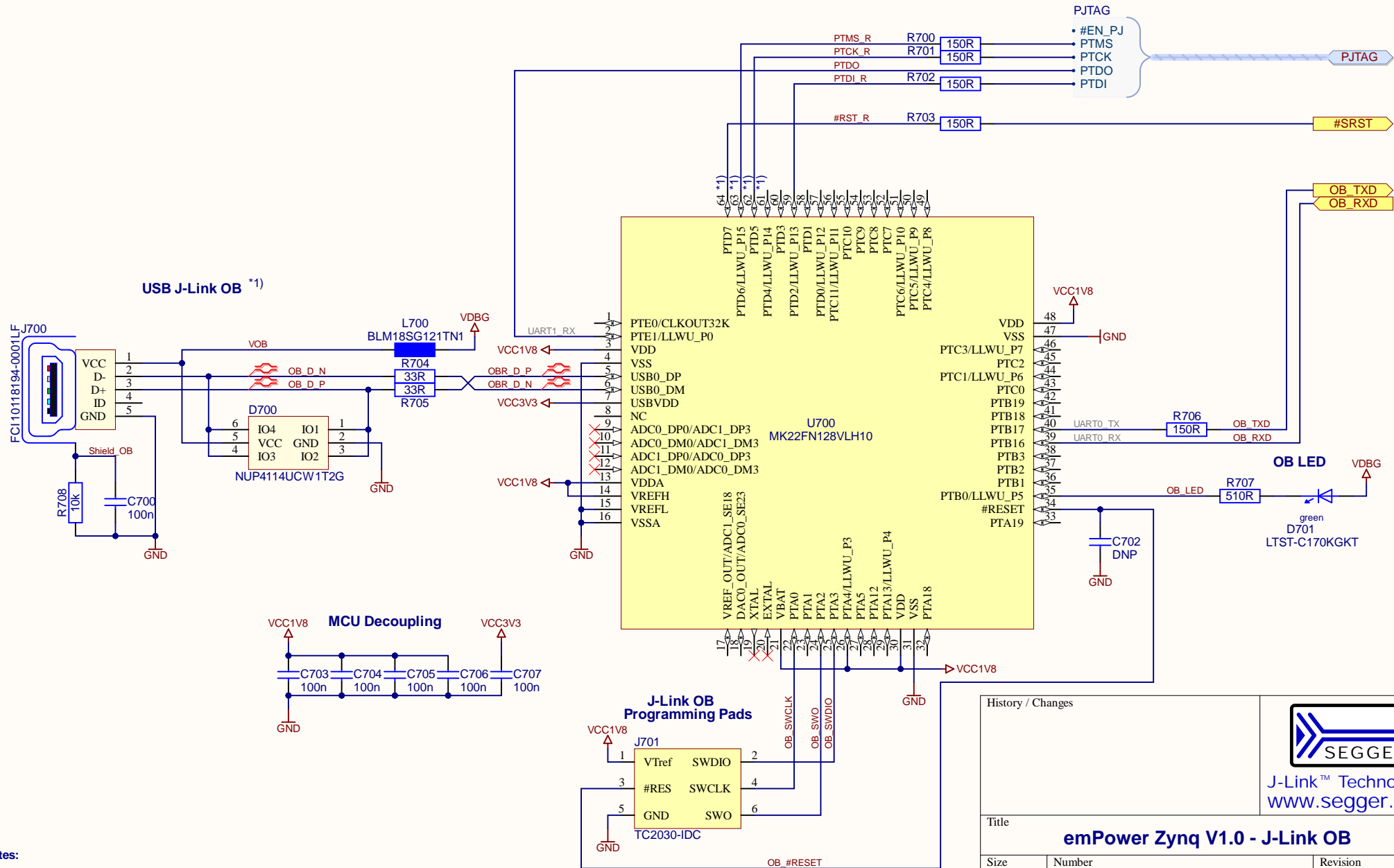
History / Changes		 J-Link™ Technology www.segger.com
Title		
emPower Zynq V1.0 - USB, GbE		
Size A3	Number -	Revision Rev. A
Date: 190702	Sheet 4 / 7	
File: Sheet04_USB_GbE_WEB.SchDoc	Drawn: VK	



History / Changes		 J-Link™ Technology www.segger.com
Title		
emPower Zynq V1.0 - USBH		
Size A3	Number -	Revision Rev. A
Date: 190702		Sheet 5 / 7
File: Sheet05_USBH_WEB.SchDoc		Drawn: VK




History / Changes		 J-Link™ Technology www.segger.com			
Title				emPower Zynq V1.0 - Power Supply	
Size	A3	Number	-	Revision	Rev. A
Date:	190702	Sheet	6 / 7	Drawn:	VK
File:	Sheet06_Power_WEB.SchDoc				



Notes:

*1) Do not power the board simultaneously by the J-Link OB connector and the main debug/trace connector!

History / Changes		 J-Link™ Technology www.segger.com
Title		
emPower Zynq V1.0 - J-Link OB		
Size	Number	Revision
A4	-	Rev. A
Date: 190702		Sheet 7 / 7
File: Sheet07_JLinkOB_WEB.SchDoc		Drawn: VK